CLAIMS

What is claimed is:

1. A method for hardening at least a portion of a gate oxide layer on a substrate, comprising:

forming an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer;

partially hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment;

forming a second resist over at least a portion of the oxide layer;

patterning the second resist to create at least one exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one non-hardened area within the oxide layer.

2. The method of claim 1, wherein the substrate comprises a silicon substrate.

3. The method of claim 2, wherein forming an oxide layer over at least a portion of the substrate comprises thermally growing an oxide layer.

4. The method of claim 1, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

5. The method of claim 4, wherein using the high density plasma remote plasma nitrogen hardening treatment comprises using a process run for in the range of approximately 1 second to approximately 30 seconds at a temperature of between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

6. The method of claim 1, wherein forming the oxide layer over at least a portion of the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å.

7. The method of claim 1, wherein patterning the resist to create at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

8. A method for fabricating an integrated circuit device including N-channel and P-channel devices having selectively hardened gate oxides on a substrate, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

conducting a first remote plasma nitrogen treatment to create at least one partially hardened area within the oxide layer and at least one non-hardened area within the oxide layer;

stripping the first resist;

growing at least a portion of the at least one non-hardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

conducting a second remote plasma nitrogen treatment to create at least one second hardened area and at least one second non-hardened area within the at least one thick area of the oxide layer.

9. The method of claim 8, wherein the substrate comprises a silicon substrate and forming the oxide layer over at least a portion of the substrate comprises thermally growing the oxide layer from the silicon substrate.

10. The method of claim 8, wherein conducting the first remote plasma nitrogen treatment to create at least one hardened area within the oxide layer and at least one non-hardened area within the oxide layer comprises conducting a high-density plasma remote plasma nitrogen treatment.

11. The method of claim 10, wherein conducting the high density plasma remote plasma nitrogen treatment comprises conducting a process run for approximately 1 second to approximately 10 seconds at between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

12. The method of claim 10, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å and growing at least a portion of the at least one non-hardened area within the oxide layer using the thermal oxidation process to form at least one thick area within the oxide layer comprises growing at least a portion of the at least one non-hardened area to a thickness of about 50Å to about 70Å.

13. The method of claim 8, further comprising processing the substrate and the oxide layer to produce an integrated circuit device including at least one P-channel device including a hardened gate oxide and at least one N-channel device including a non-hardened gate oxide.

14. A method for fabricating an integrated circuit device including N-channel and P-channel devices on a substrate, each N-channel and P-channel device having selectively hardened gate oxides, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

conducting a first remote plasma nitrogen hardening treatment to create at least one partially hardened area within the oxide layer and at least one non-hardened area within the oxide layer;

stripping the first resist;

growing at least a portion of the at least one non-hardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one second non-hardened area within the at least one thick area of the oxide layer.

15. A method for fabricating a dynamic random access memory device on a substrate comprising:

forming an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer;

partially hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment;

processing the substrate and the oxide layer to create at least one P-channel device having a hardened oxide and an array of N-channel devices, each of the N-channel devices included within the array having a non-hardened gate oxide;

forming a second resist over at least a portion within the oxide layer;

patterning the second resist to create at least one exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one non-hardened area within the oxide layer.

16. The method of claim 15, wherein the substrate comprises a silicon substrate and forming an oxide layer over the substrate comprises growing an oxide layer from the silicon substrate.

17. The method of claim 15, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

18. The method of claim 17, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run for approximately 1 second to approximately 30 seconds at between about 30° C and about 90° C using about 800 watts to about 3000 watts of power.

19. The method of claim 15, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å.

20. The method of claim 15, wherein patterning the resist to create at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

21. A method for hardening at least a portion of a gate oxide layer on a substrate, comprising:

forming an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer;

partially hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment forming a partially hardened oxide layer having a first thickness;

forming a second resist over at least a portion of the oxide layer;

patterning the second resist to create at least one exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area having a second thickness and at least one non-hardened area within the oxide layer.

22. The method of claim 21, wherein the substrate comprises a silicon substrate.

23. The method of claim 22, wherein forming an oxide layer over at least a portion of the substrate comprises thermally growing an oxide layer.

24. The method of claim 21, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

25. The method of claim 24, wherein using the high density plasma remote plasma nitrogen hardening treatment comprises using a process run for in the range of approximately 1 second to approximately 30 seconds at a temperature of between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

26. The method of claim 21, wherein forming the oxide layer over at least a portion of the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å.

27. The method of claim 21, wherein patterning the resist to create at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

28. A method for fabricating an integrated circuit device including N-channel and P-channel devices having selectively hardened gate oxides on a substrate, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

conducting a first remote plasma nitrogen treatment to create at least one partially hardened area within the oxide layer having a first thickness and at least one non-hardened area having a first thickness within the oxide layer;

stripping the first resist;

growing at least a portion of the at least one non-hardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

conducting a second remote plasma nitrogen treatment to create at least one second hardened area having another thickness and at least one second non-hardened area within the at least one thick area of the oxide layer.

29. The method of claim 28, wherein the substrate comprises a silicon substrate and forming the oxide layer over at least a portion of the substrate comprises thermally growing the oxide layer from the silicon substrate.

30. The method of claim 28, wherein conducting the first remote plasma nitrogen treatment to create at least one hardened area within the oxide layer and at least one non-hardened area within the oxide layer comprises conducting a high-density plasma remote plasma nitrogen treatment.

31. The method of claim 30, wherein conducting the high density plasma remote plasma nitrogen treatment comprises conducting a process run for approximately 1 second to approximately 10 seconds at between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

32. The method of claim 28, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å and growing at least a portion of the at least one non-hardened area within the oxide layer using the thermal oxidation process to form at least one thick area within the oxide layer comprises growing at least a portion of the at least one non-hardened area to a thickness of about 50Å to about 70Å.

33. The method of claim 28, further comprising processing the substrate and the oxide layer to produce an integrated circuit device including at least one P-channel device including a hardened gate oxide and at least one N-channel device including a non-hardened gate oxide.

34. A method for fabricating an integrated circuit device including N-channel and P-channel devices on a substrate, each N-channel and P-channel device having selectively hardened gate oxides, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

conducting a first remote plasma nitrogen hardening treatment to create at least one partially hardened area within the oxide layer having a first thickness and at least one non-hardened area within the oxide layer;

stripping the first resist;

growing at least a portion of the at least one non-hardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer having a second thickness;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one second non-hardened area within the at least one thick area of the oxide layer.

35. A method for fabricating a dynamic random access memory device on a substrate comprising:

forming an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer having a first thickness;

partially hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment;

processing the substrate and the oxide layer to create at least one P-channel device having a hardened oxide and an array of N-channel devices, each of the N-channel devices included within the array having a non-hardened gate oxide;

forming a second resist over at least a portion within the oxide layer;

patterning the second resist to create at least one exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area having a second thickness and at least one non-hardened area within the oxide layer.

36. The method of claim 35, wherein the substrate comprises a silicon substrate and forming an oxide layer over the substrate comprises growing an oxide layer from the silicon substrate.

37. The method of claim 35, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

38. The method of claim 37, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run for approximately 1 second to approximately 30 seconds at between about 30° C and about 90° C using about 800 watts to about 3000 watts of power.

39. The method of claim 35, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30Å to about 50Å.

40. The method of claim 35, wherein patterning the resist to create at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.